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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,246	INOUE ET AL.	
	Examiner	Art Unit	
	ABDULLAH AL KAWSAR	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02/20/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :04/24/2006, 08/24/2006, 12/31/2007, 01/30/2008.

DETAILED ACTION

1. Claims 1-50 are pending.

Double Patenting

2. The non-statutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In *re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

3. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

4. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1, 2 and 3 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 10 and 12 of copending Application No. 10/783238. Although the conflicting claims are not identical, they are not patentably distinct from each other because both systems comprise substantially the same elements. For

example, Claims 1and 2 functions performed by the steps of the instant application are the same and obvious as the steps of claim 10 of copending application No. 10/783238 (Storing the processor tasks in a shared memory/processor tasks be copied from the shared memory that may be accessed by a plurality of processing units of the multiprocessor computing system/ Plurality of processing units that may access a shared memory, permitting the processing units to determine which of the processor tasks should be executed based on priorities of the processor/ the processing units select processor tasks from shared memory for execution based on priority levels of the processor tasks. The processor tasks that are executed are copied from the shared memory/ providing that the selected processor tasks be copied from the shared memory and executed by one or more of the processing units.). The difference is the substitution of execution based on priority in the present application with the preemptively replaced the lower priority task with the higher priority. It would have been obvious to one of the ordinary skill in the art to preemptively replace the lower priority task to be able to execute the task in order of priority.

6. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented. Double patenting rejection remains until a proper terminal disclaimer is filed.

Claim Objections

7. Claim 44 is objected to because of the following informalities: Claim 44 does not end appropriately, please replace ";" with "." at the end of claim 44. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-50 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following claim languages are not clearly understood and indefinite:

i. Claim 1, line 1 it is not clearly understood the meaning of "processor tasks", are they tasks meant to be executed on a specific processor or are they tasks that are waiting in the queue to be executed or are they tasks that are being executed. Furthermore, it is unclear where "processor tasks" reside. Line 3, "may access", it is unclear whether or not the processing units access the shared memory. The claim language is broad and indefinite.

ii. Claims 4, 19, 26 29 and 43 has similar deficiencies as claim 1 above.

iii. Claim 2, line 2 recites "copied from the shared memory" it is unclear where it is being copied to from the shared memory.

iv. Claims 5, 8, 27, 33 have similar deficiencies as claim 2 above.

v. Claim 7 it is unclear how "task table" and "task queue" related to each other and what is the difference between them in terms of task listing (i.e. copying the task from table to queue in a specific order or group?) Lines 10 recite "the list" it is unclear which list is being used to execute that task (i.e. the task queue list or task table list?).

vi. Claims 20, 32 and 45 has similar deficiencies as claim 7 above.

vii. Claim 11, line 5 recites "copying task queue and table" it is unclear if the entire task table and queue is being copied or only the entry related to the processor and why both are being copied (i.e. queue and table has different type of task entry? What is the difference?). Lines 10-12 the processor task is copied to the local memory which was already copied to the local memory in lines 5-7, it is unclear why the tasks are being copied twice.

viii. Claims 21, 36 and 46 has similar deficiencies as claim 11 above.

ix. Claim 13, line 2 recite " the list" it is unclear which list is that (i.e. queue or table list?).

x. Claim 18 it is unclear where the task table is being copied to from the shared memory (i.e. to another processor's local memory for a different task execution?).

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-6 and 26-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirayama (Hirayama) US Patent No. 5592671.

12. As per claim 1, Hirayama teaches the invention as claimed including a method of managing processor tasks in a multi-processor computing system(abstract, lines 1-3), comprising:

storing the processor tasks in a shared memory that may be accessed by a plurality of processing units of the multi-processor computing system (col 2, lines 54-62); and

permitting the processing units to determine which of the processor tasks should be executed based on priorities of the processor tasks (col 1 lines 64-67 through col 3, lines 1-7).

13. As per claim 2, Hirayama teaches the processor tasks that are executed are copied from the shared memory (col 5, lines 33-42).

14. As per claim 3, Hirayama teaches the processing units comprise a main processing unit and a plurality of sub-processing units and the sub-processing units access the processor tasks in the shared memory (figure 1).

15. As per claim 4, Hirayama teaches the invention as claimed including a method of managing processor tasks in a multi-processor computing system(abstract, lines 1-3), comprising:

storing the processor tasks in a shared memory that may be accessed by a plurality of processing units of the multi-processor computing system(col 2, lines 54-62);

storing a task table in the shared memory, the task table including a task table entry associated with each of the processor tasks (figure 1; col 2, lines 58-62);

linking at least some of the task table entries together to achieve at least one list of processor tasks to be invoked in hierarchical order (figure 1; figure 3; col 4, lines 27-32); and

permitting the processing units to use the task table to determine which of the processor tasks should be executed in accordance with the list of processor tasks (col 2, lines 64-67).

16. As per claim 5, Hirayama teaches the processor tasks that are executed are copied from the shared memory (col 4, lines 53-58).

17. As per claim 6, Hirayama teaches each of the task table entries includes at least one of (col 2, lines 58-61):

(i) an indication as to whether the associated processor task is ready to be executed by one or more of the processing units (col 4, lines 43-47);

(ii) an indication as to a priority level of the associated processor task (col 3, lines 18-22);

(iii) a pointer to a previous task table entry in the list of task table entries (a previous pointer); and

(iv) a pointer to a next task table entry in the list of task table entries (figure 3).

18. As per claim 29, Hirayama teaches a multi-processor apparatus, comprising:

a plurality of processing units, each processing unit including a local memory in which to execute processor tasks (col 5, lines 1-3; col 6, lines 9-14); and

a shared memory operable to store: (i) processor tasks that are ready to be executed, and (ii) a task table including a task table entry associated with each of the processor tasks, wherein the processing units are operable to use the task table to determine which of the processor tasks should be copied from the shared memory into their local memories and executed (col 2, lines 54-62; lines 64-67; col 5, lines 33-37; col 6, lines 9-16; lines 37-40).

19. As per claim 30, Hirayama teaches at least some of the task table entries are linked together to achieve at least one list of processor tasks to be invoked in hierarchical order (figure 1; figure 3; col 4, lines 27-32); and

the processing units are operable to use the linked list to determine which of the processor tasks should be copied from the shared memory and executed (col 4, lines 53-58).

20. As per claims 26-28, they have similar limitations as of claims 1-3 above. Therefore they are rejected under the same rational as of claims 1-3 above.

21. As per claim 31, it has similar limitations as of claim 6 above. Therefore it is rejected under the same rational as of claim 6 above.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 7-14, 16-22, 32-39 and 41-47 rejected under 35 U.S.C. 103(a) as being unpatentable over Hirayama(Hirayama) US Patent No. 5592671, in view of Bahr (Bahr) EP 0459931.

24. As per claim 7, Hirayama dose not specifically disclose storing a task queue in the shared memory, the task queue including at least one of a head pointer and a tail pointer, the head pointer providing an indication of a first one of the processor tasks in the list, and the tail pointer providing an indication of a last one of the processor tasks in the list; and

permitting the processing units to use the task table and the task queue to determine which of the processor tasks should be executed in accordance with the list of processor tasks.

25. However, Bahr teaches storing a task queue in the shared memory, the task queue including at least one of a head pointer and a tail pointer, the head pointer providing an indication of a first one of the processor tasks in the list, and the tail pointer providing an indication of a last one of the processor tasks in the list (col 8, lines 26-30; lines 14-16; lines 52-53); and

permitting the processing units to use the task table and the task queue to determine which of the processor tasks should be executed in accordance with the list of processor tasks (col 8, lines 4-16).

26. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Bahr into the method of Hirayama to have head and tail pointer in the task queue. The modification would have been obvious because one of the ordinary skills of the art would have implemented pointers to in the task queue to be able to track the queue and incorporate other queue with an existing queue chain for faster read/write of the queue and execution of task.

27. As per claim 8, Hirayama teaches the processor tasks that are executed are copied from the shared memory(col 5, lines 33-42).

28. As per claim 9, Bahr teaches linking respective groups of the task table entries together to produce respective lists of processor tasks, each list being in hierarchical order (col 8, lines 26-30); and

providing that the task queue includes respective task queue entries, each entry including at least one of a head pointer and a tail pointer for each of the lists of processor tasks (col 8, lines 52-58 through col 9, lines 1-6).

29. As per claim 10, Hirayama teaches each of the respective lists are associated with processor tasks of a common priority level (col 3, lines 27-30); and

the task queue includes a task queue entry for each of a plurality of priority levels of the processor tasks (col 3, lines 44-50).

30. As per claim 11, Bahr teaches the plurality of processing units includes a plurality of sub-processing units, each of the sub-processing units having local memory(abstract, lines 1-4), further comprising:

copying the task queue and the task table from the shared memory into the local memory of a given one of the sub-processing units (col 6, lines 35-43; col 9, lines 6-10col 7, lines 23-27);

searching the task queue for the head pointer to a given one of the processor tasks that is ready to be invoked (col 8, lines 11-16); and

copying the given processor task from the shared memory to the local memory of the given sub-processing unit for execution (col 8, lines 4-8; col 9, lines 53-57; col 6, lines 50-54).

31. As per claim 12, Bahr teaches the step of searching the task queue includes searching for the head pointer to a highest priority level one of the processor tasks that is ready to be invoked (col 8, lines 4-8; lines 11-16)

32. As per claim 13, Bahr teaches removing the given processor task from the list (col 1, lines 24-28).

33. As per claim 14, Bahr teaches each of the task table entries includes a pointer to a next task table entry (col 8, lines 53-56); and

the removal step includes using the next pointer of the given task table entry to change the head pointer to identify the new first processor task as being ready to be next invoked (col 8, lines 53-56; lines 14-16;).

34. As per claim 16, Bahr teaches each of the task table entries includes an indication as to whether the associated processor task is READY to be executed or is RUNNING on one or more of the sub-processing units (col 1, lines 34-43); and

the method further includes modifying the given task table entry to indicate that the given processor task is RUNNING (col 1, lines 43-47).

35. As per claim 17, Bahr teaches copying the task queue and the task table from the local memory of the given sub-processing unit into the shared memory when the given sub-processing unit has completed its use thereof (col 10, lines 41-49).

36. As per claim 18, Bahr teaches permitting the task queue and the task table to be copied from the shared memory when the given sub-processing unit has completed its use thereof (col 10, lines 41-49).

37. As per claim 19, Hirayama teaches a method of managing processor tasks in a multi-processor computing system (abstract, lines 1-3), comprising:

storing the processor tasks in a shared memory that may be accessed by a plurality of processing units of the multi-processor computing system(col 2, lines 54-62);

storing a task table in the shared memory, the task table including a task table entry associated with each of the processor tasks (figure 1; col 2, lines 58-62);

linking at least some of the task table entries together to achieve at least one list of processor tasks in hierarchical order (figure 1; figure 3; col 4, lines 27-32);

determining which of the other processor tasks should be executed next within the given processing unit by permitting the given processing unit to use the task table to make such determination(col 2, lines 64-67).

Hirayama does not specifically disclose at least initiating execution a first one of the processor tasks of the list within a given one of the processing units, wherein the first one of the processor tasks yields the given processing unit such that it is capable of executing another of the processor tasks.

However Bahr teaches at least initiating execution a first one of the processor tasks of the list within a given one of the processing units, wherein the first one of the processor tasks yields the given processing unit such that it is capable of executing another of the processor tasks (col 1, lines 24-28).

38. As per claim 20, Bahr teaches storing a task queue in the shared memory, the task queue including at least one of a head pointer and a tail pointer, the head pointer providing an indication of a new first one of the processor tasks in the list, and the tail pointer providing an

indication of a last one of the processor tasks in the list (col 7, lines 2-27; col 8 lines 14-16; lines 53-58 through col 9, lines 1-3); and

permitting the processing units to use the task table and the task queue to determine which of the processor tasks should be executed next (col 8, lines 4-8; lines 14-16)

39. As per claim 21, Bahr teaches the plurality of processing units include a plurality of sub-processing units, each of the sub-processing units having local memory, and wherein the step of determining includes(abstract, lines 1-4):

copying the task queue and the task table from the shared memory into a local memory of the given sub-processing unit (col 6, lines 35-43; col 9, lines 6-10col 7, lines 23-27); and

searching the task queue for the head pointer to the new first processor task that is ready to be invoked (col 8, lines 11-16).

40. As per claim 22, Bahr teaches adding the first processor task back into the list (col 9, lines 13-20).

41. As per claim 32-39 and 41-42, they have similar limitations as of claims 7-14 and 16-17 above. Therefore they are rejected under the same rational as of claims 7-14 and 16-17 above.

42. As per claims 43 and 45, they have similar limitations as of claims 19 and 20 above. Therefore they are rejected under the same rational as of claims 19 and 20 above.

43. As per claim 44, Hirayama teaches at least some of the task table entries are linked together to achieve at least one list of processor tasks in hierarchical order (figure 1; figure 3; col 4, lines 27-32).

44. Claims 15, 23-25, 40, 48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirayama(Hirayama) US Patent No. 5592671, in view of Bahr (Bahr) EP 0459931, in view of Arnon et al. (Arnon) US Patent No. 6321308.

45. As per claim 15, Hirayama and Bahr do not specifically disclose each of the task table entries includes a pointer to a previous task table entry; and the method further includes modifying the previous pointer of the last task table entry of the list to point to the task table entry associated with the new first processor task of the list.

46. However, Arnon teaches each of the task table entries includes a pointer to a previous task table entry (col 4, lines 49-54); and

the method further includes modifying the previous pointer of the last task table entry of the list to point to the task table entry associated with the new first processor task of the list (col 7, lines 52-62).

47. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Arnon into the combined method of Hirayama and Bahr to have a previous pointer to point to the next task table entry. The modification would have been

obvious because one of the ordinary skills of the art would have a previous and next pointer on a linked list based task table to be able to modify the pointers for add and delete operations.

48. A per claim 23, Arnon teaches each of the task table entries includes a pointer to a next task table entry and pointer to a previous task table entry (col 4, lines 49-58); and

the step of adding includes modifying the linking of the task table entries to include links to the task table entry associated with the first processor task (col 7, lines 3-7; lines 26-35).

49. As per claim 24, Arnon teaches wherein the step of modifying the linking of the task table entries includes linking the task table entry associated with the first processor task between a prior task table entry and a following task table entry that were previously linked to one another (col 7, lines 24-32).

50. As per claim 25, Arnon teaches modifying the next pointer of the prior task table entry to point to the task table associated with the first processor task (col 7, lines 39-41);

modifying the previous pointer of the task table entry associated with the first processor task to point to the prior task table entry (col 7, lines 38-39);

modifying the next pointer of the task table entry associated with the first processor task to point to the following task table entry (col 7, lines 42-45); and

modifying the previous pointer of the following task table entry to point to the task table entry associated with the first processor task (col 7, lines 45-49).

51. As per claim 40, it has similar limitations as of claim 15 above. Therefore it is rejected under the same rational as of claim 15 above.

52. As per claims 48-50, they have similar limitations as of claims 23-25 above. Therefore they are rejected under the same rational as of claims 23-25 above.

Conclusion

53. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH AL KAWSAR whose telephone number is (571)270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

54. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

55. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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